



Novel Technique to Reduce Substrate Tilt & Improve Bondline Control between AlN Substrate and AlSiC Baseplate in IGBT Modules

Authored by: Karthik Vijay, Indium Corporation; and James Booth, Paul Mumby-Croft, Matthew Packwood, Kim Evans, and Andy Dai, Dynex Semiconductor Ltd.

Abstract

Bondline control, which is the use of spacers or standoffs applied to a power module's baseplate to achieve a homogenous solder layer, is a well-understood technology employed by most power semiconductor manufacturers. It is understood that an inhomogeneous solder layer can lead to early device failure caused by cracking and delamination of the solder during thermal cycling, and that spacer technology such as stitched wire bonds for AlSiC baseplates or stamped "bumps" on copper baseplates can inhibit this behavior and increase joint lifetime.

This paper presents a novel alternative method of achieving bondline control on AlSiC baseplates while offering a drop-in solution with no additional manufacturing steps or capital investment costs: a solder preform engineered with an embedded metal mesh across the area of the preform. Samples were made to evaluate the thermal fatigue resistance of this technology in comparison to both the traditional wire bond method and samples made without any bondline control. Active metal braze Cu-AlN-Cu substrates were soldered to 140mm x 70mm AlSiC baseplates for these trials with each bondline variant. The samples were then temperature-cycled at a ΔT of 200K, and analyzed by scanning acoustic microscopy every 200 cycles. Cracking and solder layer delamination were observed at 600 cycles for the samples without bondline control and at 800 cycles for the samples with Al wire bonds; no sign of thermal fatigue was witnessed on the samples with the embedded metal mesh. The embedded metal mesh samples showed the least co-planarity deviation and superior reliability results to the Al wire bond method with the added advantage of no additional process steps.

Introduction

Large area solder joints in multi-chip power semiconductor packages experience fatigue caused by the periodic straining of the interconnection layers during thermal excursions while the device is operational. These stresses lead to delamination and cracks within the solder layer after many thermal cycles, which increase the module to heat-sink thermal resistance and ultimately lead to early device failure [2].

Cracking and solder layer delamination occurs earlier in inhomogeneous solder joints due to stress concentration at thinner areas of the joint. Figure 1 shows how crack length within the solder joint increases greatly with solder layers thinner than 200 μm . This figure illustrates how tilted samples where part of the joint is <200 μm is more susceptible to cracking and delamination.

KARTHIK VIJAY



Karthik Vijay is based in the UK and is responsible for technology programs and technical support for our customers in Europe. Prior to this, he was based in San Jose, California and was responsible for applications support for customers on the North American West Coast. His expertise is focused on engineered solders (power electronics), solder paste, thermal interface materials, and semiconductor-grade electronics materials.

Karthik joined Indium Corporation in 2003 and has over 15 years of experience in electronics assembly. He is active in several industry organizations, including IMAPS, SMTA, and has presented at several industry forums and conferences nationally and internationally.

email: kvijay@indium.com

Full biography:

www.indium.com/biographies

The advent of spacer technology allows control of the solder joint thickness for a given solder volume by reducing substrate tilt to achieve a homogenous solder layer as Figure 2 demonstrates. This is most commonly done in power semiconductor modules by stitch bonding aluminium wire of a desired diameter to an AlSiC baseplate: for copper baseplate modules, copper “bumps” can be stamped in the component (Figure 3).

The use of spacers in large area solder joints increases the joint lifetime by allowing for homogenous delamination. This occurs at a much slower rate than inhomogeneous delamination caused by substrate tilt [1-2]. This technology is well documented and employed today in power module assembly but this technique results in a high cost of ownership due to extra process steps and capital equipment costs.

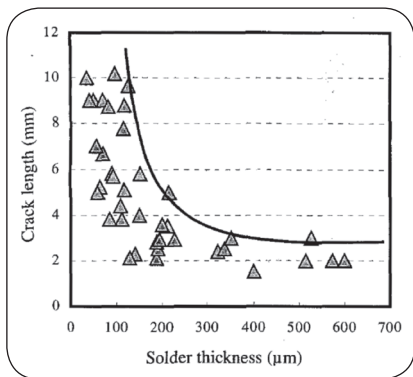


Figure 1. Correlation between solder joint thickness and induced crack length after thermal cycling [1].

An alternative solution to achieving a homogenous solder layer is proposed by using a solder preform engineered with an embedded metal mesh. In the same way as the traditional wire bond method, when the solder melts during reflow the metal mesh remains intact and serves to maintain a uniform bondline thickness. As

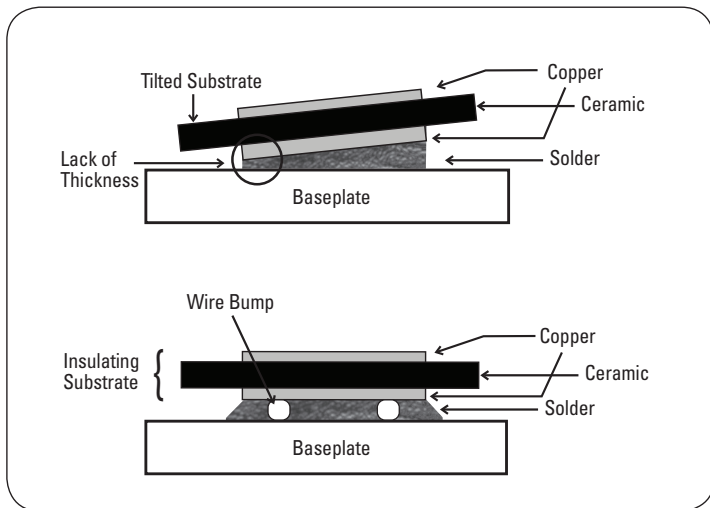


Figure 2. Substrate tilt example (top) and solution using wire bonds to achieve bondline uniformity (bottom) [1].

well as the obvious reduction in manufacturing time by the advent of a drop-in solution to achieving bondline homogeneity, the lifetime of this novel technique is evaluated against the traditional aluminium stitch bond method.

Sample Preparation

To evaluate the lifetime of the embedded metal mesh preform, sample modules were made and evaluated against the traditional wire bond method for achieving a homogenous solder layer. These samples were also compared to reference modules with no bondline control; four of each variant was tested. The samples were then temperature cycled with a ΔT of 200K, and cracking and delamination of the solder layer was monitored by scanning acoustic microscopy every 200 cycles.

Module assembly consisted of soldering ceramic AlN substrates (with Cu metallization) to 140mm x 70mm AlSiC baseplates using 200µm SnSb5 solder preforms. The samples with the embedded metal mesh consisted of a 200µm mesh with a 225µm net solder thickness. The samples with aluminium stitch bonds used 200µm diameter wire. The net height, however, is reduced to approximately 180µm due to the compression of the wire caused by the bond tool (Figure 4). These were compared to 200µm thick preforms with no bondline control.

200µm is the targeted bondline thickness as this offers the lowest thermal resistance without suffering from increased strain. Figure 5 illustrates how the normalized strain (non-dimensional strain normalized by the equivalent plastic strain) increases rapidly at thickness <200µm, yet at thicknesses up to 600µm the normalized strain barely alters. This effect is also shown in Figure 1 as the increased strain on the solder joint promotes crack propagation [1].

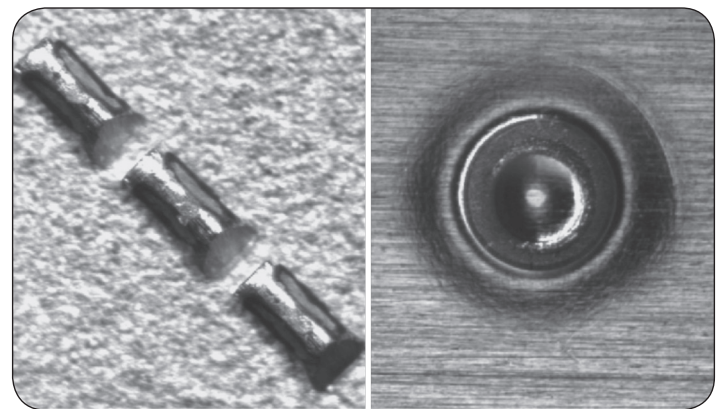


Figure 3. Traditional bondline control methods, aluminium wire bonds on AlSiC baseplate (left), and stamped “bump” in copper baseplate (right).

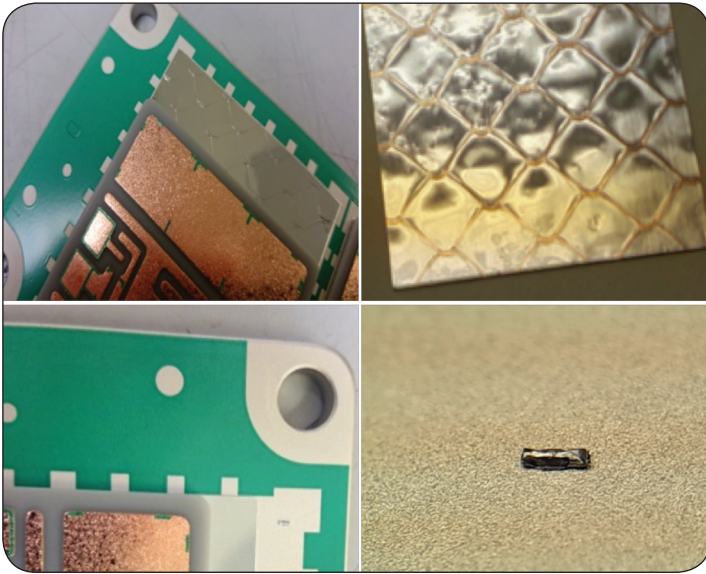


Figure 4. Assembly images showing sample soldered with metal mesh preform (top) and sample with wire bond spacer (bottom).

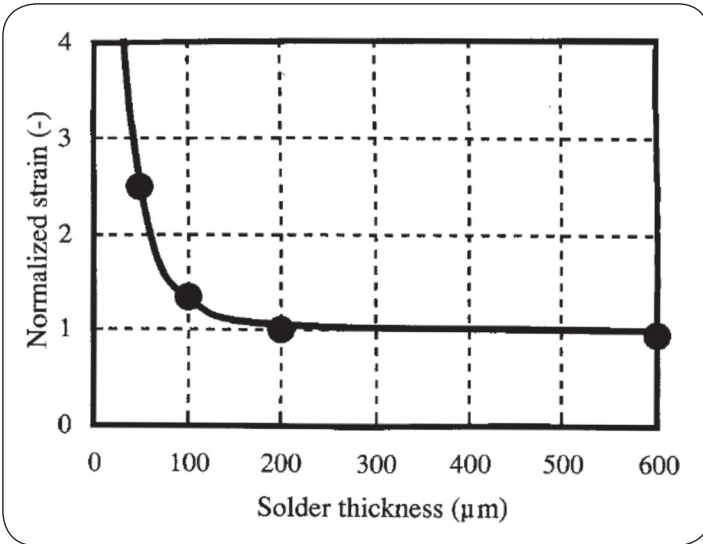


Figure 5. Correlation between solder thickness and the non-dimensional strain normalized by the equivalent plastic strain [1].

Following the assembly of the samples, one of each sample type underwent a laser surface profiling scan to determine the substrate tilt prior to thermal cycling tests. This was determined as the mean height variation across the top of the substrate at four points; the maximum deflection was also measured. The sample with the embedded metal mesh shows the least co-planarity deviation (smallest ΔZ) at $52.5\mu\text{m}$ and a maximum deflection of $\sim 60\mu\text{m}$ (Figure 6). This was followed by the wire bonded sample at $56.5\mu\text{m}$ with a maximum deflection at $\sim 70\mu\text{m}$ (Figure 7) and

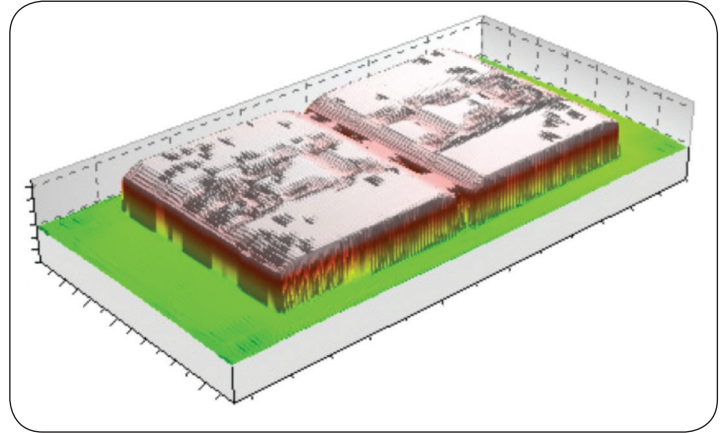


Figure 6. Sample with embedded metal mesh; mean co-planarity deviation = $52.5\mu\text{m}$, maximum deflection = $60\mu\text{m}$.

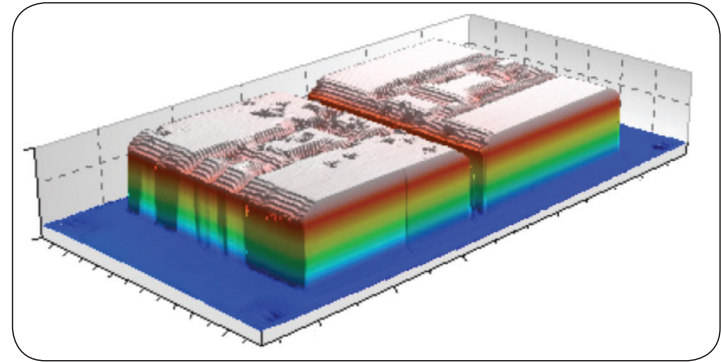


Figure 7. Sample with aluminium stitch bonds; mean co-planarity deviation = $56.5\mu\text{m}$, maximum deflection = $70\mu\text{m}$.

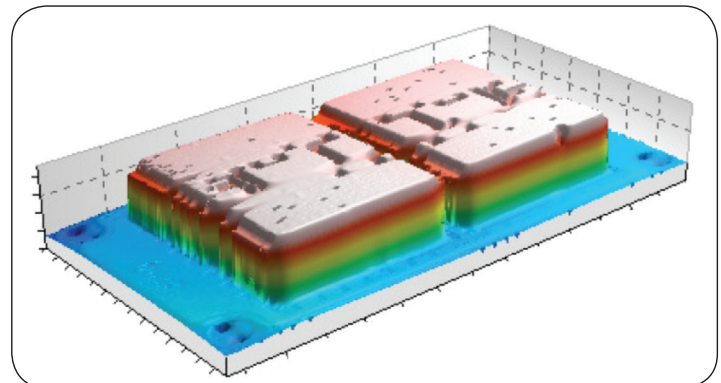


Figure 8. Sample with no bondline control; mean co-planarity deviation = $67.5\mu\text{m}$ maximum deflection = $90\mu\text{m}$.

finally the sample without bondline control at $67.5\mu\text{m}$ and a maximum deflection of $\sim 90\mu\text{m}$ (Figure 8). It is noticed that on all samples, the substrates are tilted inward toward the baseplate, owing to the concave shape of the baseplate.

Thermal Cycling

Samples were thermal cycled using a Vötsch VT 7012 S3 chamber-to-chamber thermal cycler. The samples were cycled from -50°C to 150°C under the following conditions (Figure 9):

$$t_{\text{dwell}} = 1 \text{ hour} \quad T_{\text{s(max)}} = 150^{\circ}\text{C}$$

$$t_{\text{transition}} = 30 \text{ seconds} \quad T_{\text{s(min)}} = -50^{\circ}\text{C}$$

$$\Delta T = 200\text{K}$$

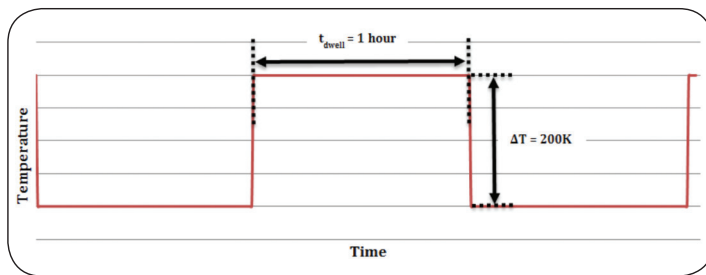


Figure 9. Representative temperature profile for thermal cycling test conditions.

Results

Figure 10 shows the initial SAM images at zero cycles of the baseplate/solder interface for all three techniques. Delamination of the solder layer is witnessed as bright reflections emanating from the edges of the solder layer. No delamination was witnessed at 200 and 400 cycles for all bondline variants; however, Figure 11 shows the metal mesh in the preform highlighted after 400 cycles. This is likely due to the expansion of the metal mesh within the solder; however, this expansion was not shown to increase with further thermal cycling. Figure 12 (c) shows bright reflections appearing at the edges of the solder after 600 thermal cycles for the samples with no bondline control. The samples with the embedded metal mesh showed no signs of delamination or solder layer cracking.

The sample shown in Figure 12 (c) and other samples made with no bondline control exhibited similar behavior at the same number of thermal cycles. These defects did not drastically increase at 800 cycles (Figure 13). Cracking was witnessed in the secondary SAM gate reflecting the substrate/solder layer by showing bright reflections, which indicated cracking. This was apparent with all samples tested without bondline control as shown in Figure 14. Figure 15 (a) shows signs of cracking with the samples made with Al wire bonds. These appear at the same location where the solder layer is at its thinnest due to the concave nature of the baseplate. No signs of cracking or delamination after 800 cycles for samples with the embedded metal mesh is observed, as shown in Figure 15 (b).

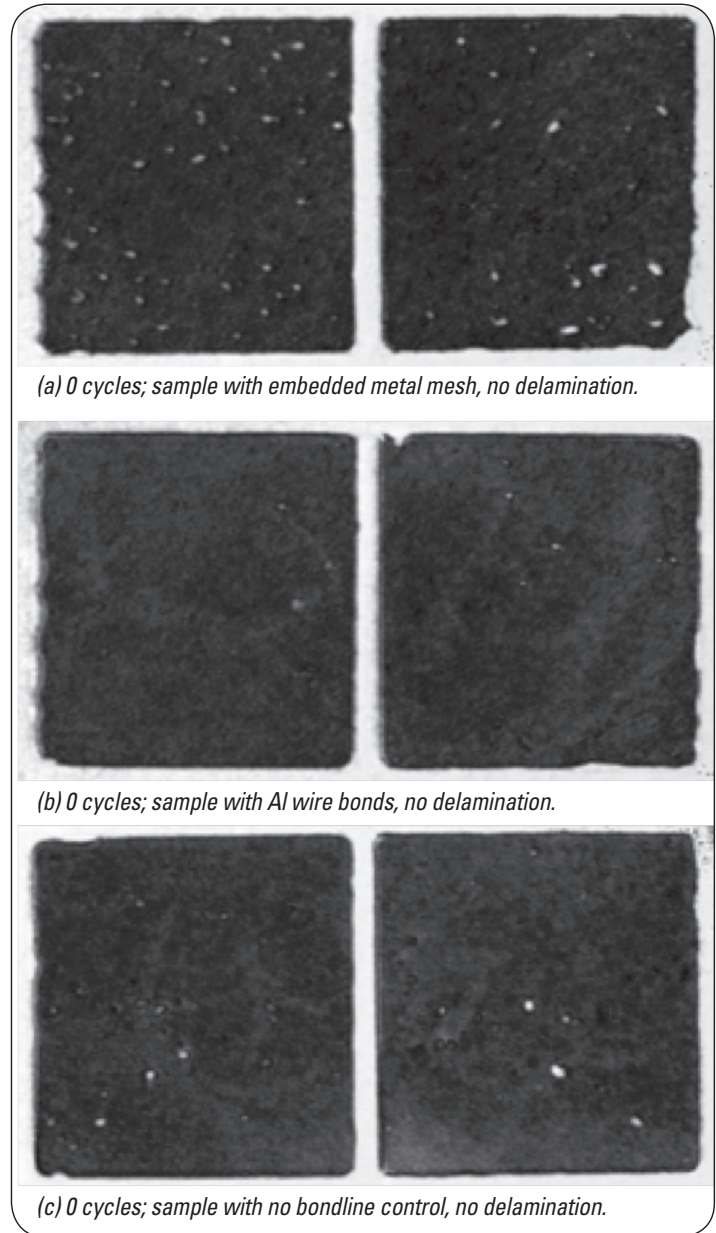


Figure 10. Initial SAM results at zero cycles.

Summary and Conclusion

A novel technique to prevent substrate tilt and maintain a homogenous 200µm solder layer using an embedded metal mesh was evaluated and compared to the traditional aluminium stitch bond technique for AlSiC baseplate modules. Samples were evaluated against aluminium stitch bonded modules and modules with no bondline control.

Following module assembly, the top surface of the substrates underwent a surface profile scan to determine the substrate

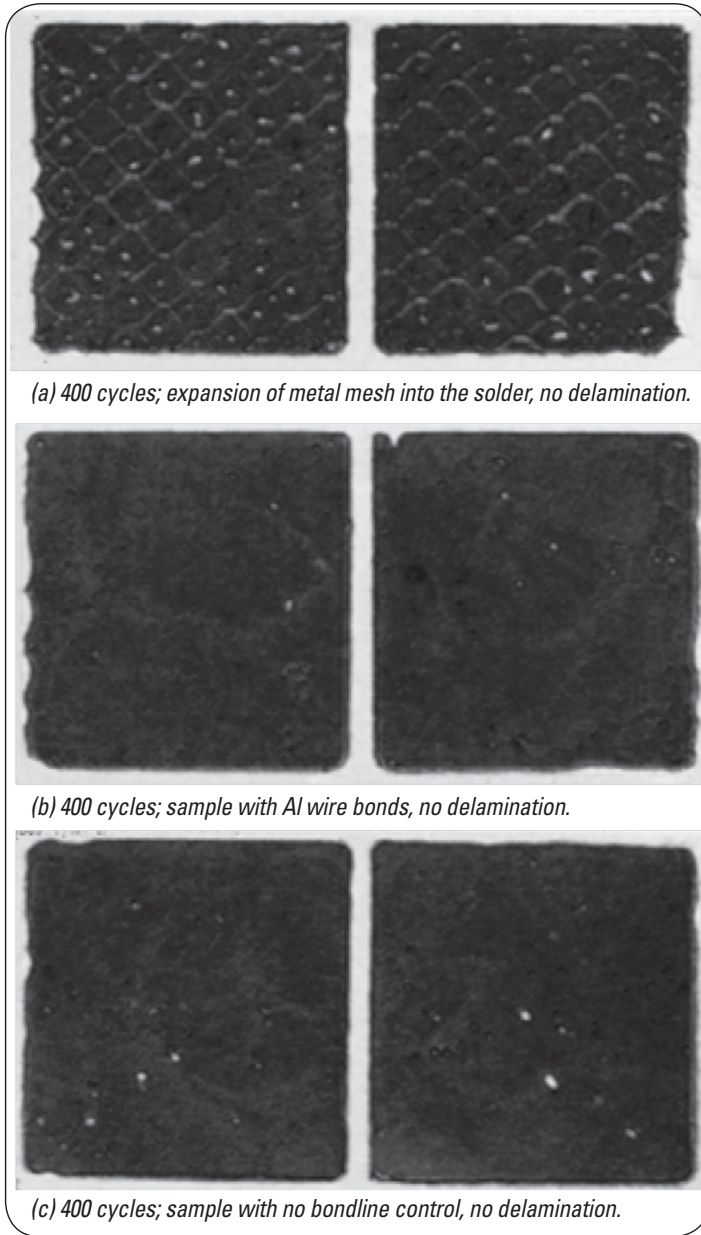


Figure 11. SAM images after 400 thermal cycles.

tilt. The mean co-planarity deviation revealed the sample with the embedded metal mesh had the lowest co-planarity deviation of 52.5 μ m and the sample with no bondline control had the highest deviation of 67.5 μ m. Additionally, the maximum recorded values between two points over 40mm recorded the maximum tilt on the sample with no bondline control to be ~90 μ m. The values for the maximum deviation between two points for the other samples were ~60 μ m for the embedded metal mesh sample, and ~70 μ m for the sample with aluminium wire bonds.

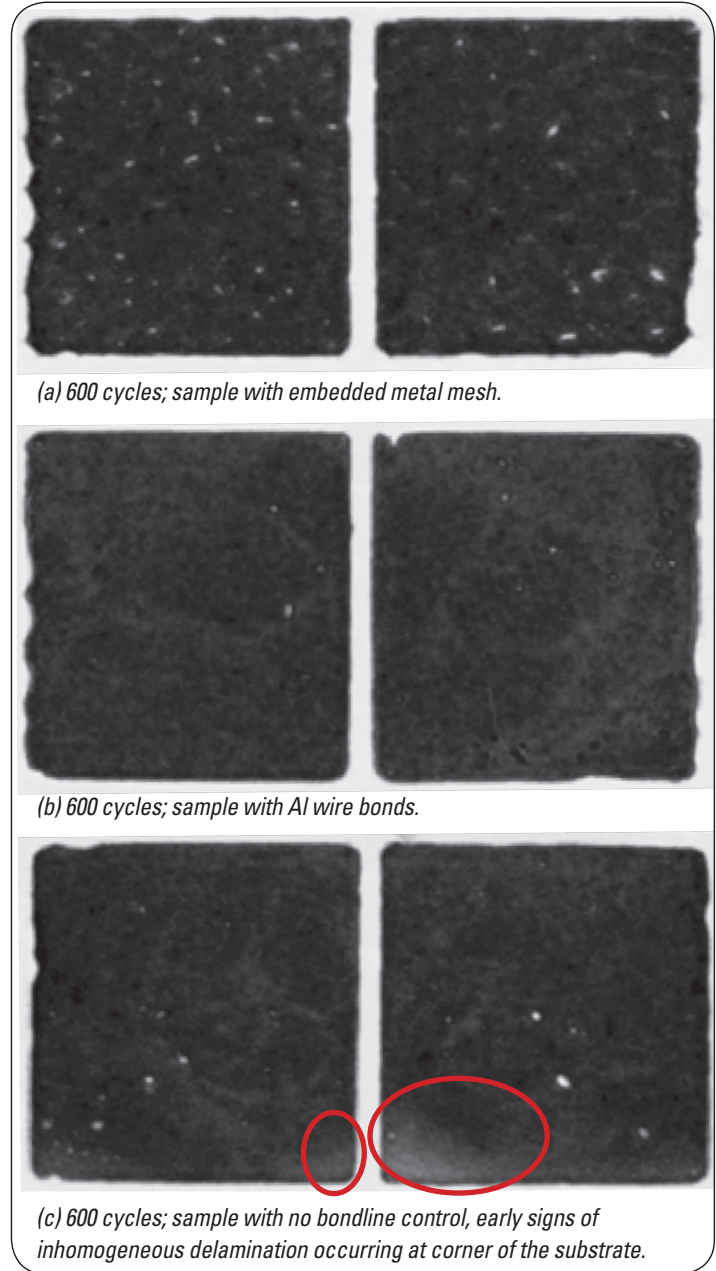


Figure 12. SAM results after 600 cycles.

Temperature cycling tests revealed solder layer delamination and cracking of the solder joint following the substrate tilt (as was measured before cycling). The samples with no bondline control showed cracking at 600 thermal cycles at the tilted side with a difference of ~90 μ m, the lowest side of which emanated cracking and delamination. The samples with Al wire bonds showed signs of cracking at 800 thermal cycles with some but not all samples; cracks appeared at the thinner end of the solder joint, i.e., the center of the baseplate. No cracks or solder delamination were seen for the samples with the embedded metal mesh.

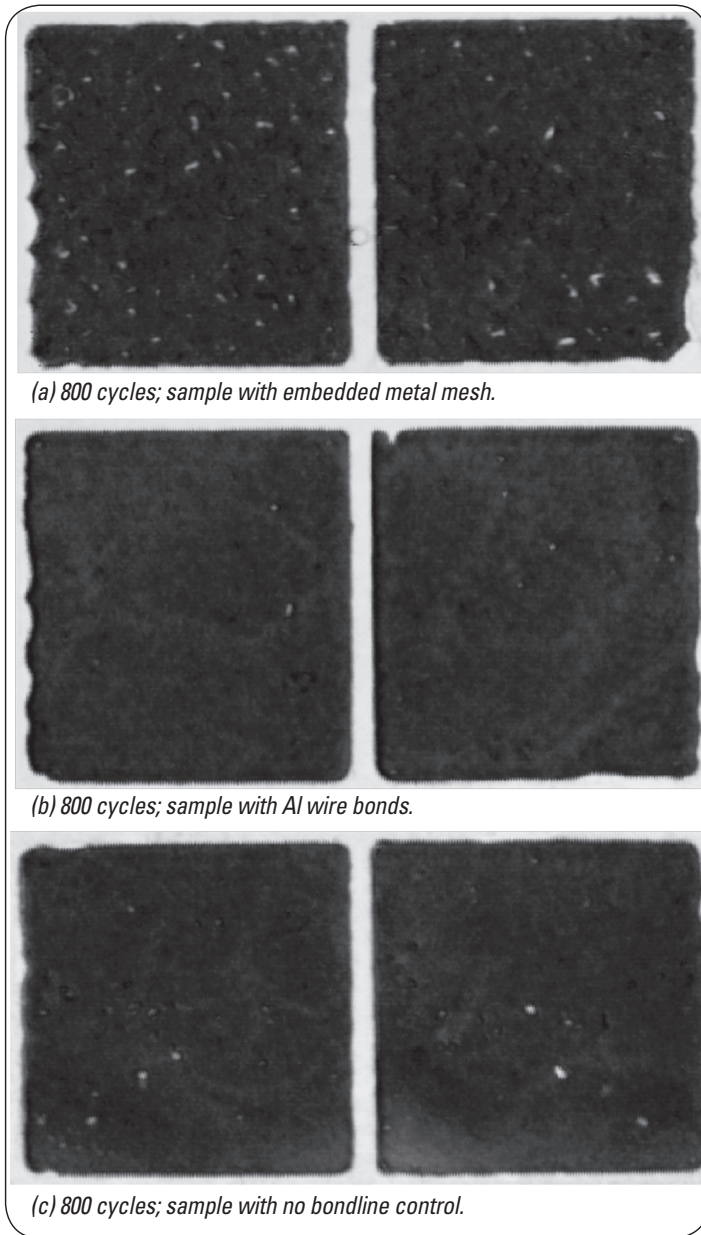


Figure 13. SAM results after 800 cycles.

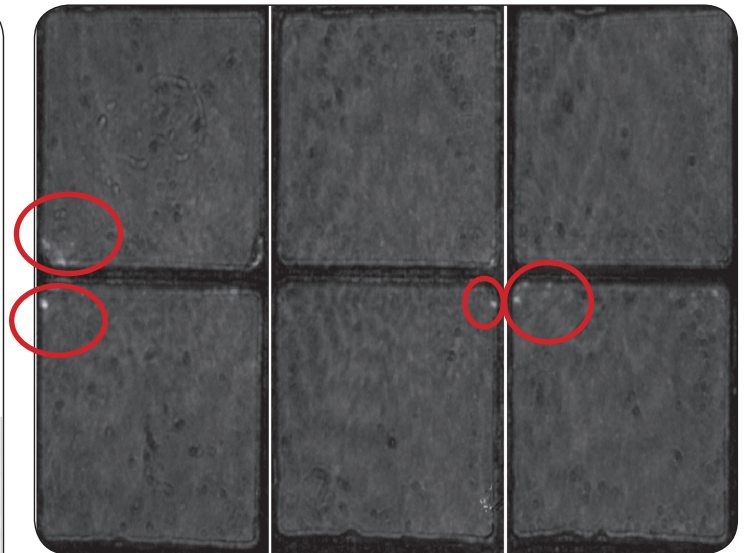


Figure 14. Secondary SAM gate highlighting cracks in the solder layer after 600 thermal cycles for samples made with no bondline control.

While the effect of bondline control has already been studied and shown to improve joint lifetime in power modules, this paper presents an alternative solution to the aluminium stitch bonding method. The metal mesh within the solder preform suppressed solder fatigue up to 800 cycles and showed a greater reliability to the traditional wire bond method. The presence of the metal mesh became apparent after 400 cycles, though this effect appeared to get no worse with an increasing number of cycles.

The embedded metal mesh preform offers a drop-in and cost-effective solution to achieving bondline homogeneity without additional process steps or costly capital investment for wire bonding spacers (eliminating the need for dedicated wire bonders, maintenance, fixtures, etc.). After 800 thermal cycles, the embedded metal mesh preform showed no signs of cracking or solder layer delamination. In this test, this method showed improved reliability to the Al wire bond method.

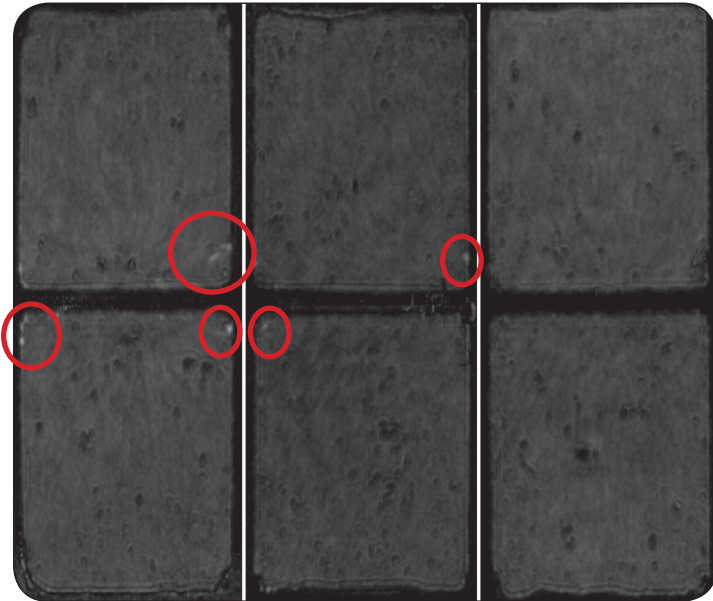


Figure 15. (a) 800 cycles; secondary SAM gate highlighting cracks in the solder layer for samples with Al wire bonds.

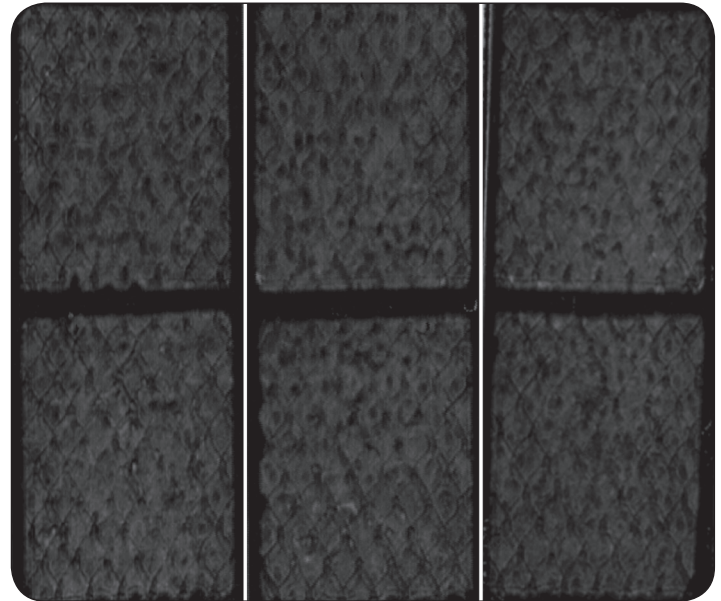


Figure 15. (b) 800 cycles; secondary SAM gate showing no signs of cracking/delamination for the samples with the embedded metal mesh.

Acknowledgments

The authors would like to thank Dr. Steve Jones for his contribution to this research.

References

1. K. Hayashi & G. Izuta, "Improvement of Fatigue Life of Solder Joints by Thickness Control of Solder with Wire Bump Technique," ECTC 2002.
2. K. Guth & P. Mahnke, "Improving the Thermal Reliability of Large Area Solder Joints in IGBT Power Modules," Integrated Power Systems (CIPS) 2006.
3. L. Mills & K. Vijay, "InFORMS vs the Trimmed Wirebond Technique to Achieve Uniform Bondline Control Between Substrate and Baseplate," PCIM Europe 2015.

First presented at PCIM 2016, May 2016, Nuremberg, Germany.